Claims

[c1] 1. An active device array structure for rapidly twisting the alignment of liquid crystal molecules from a splay state to a bend state, the active device array structure comprising:

a base plate;

a plurality of gate lines disposed over the base plate;

a plurality of data lines disposed over the base plate, wherein a pixel area is formed between any two adjacent gate lines and any two adjacent data lines;

a plurality of active devices disposed over the base plate, wherein each active device isformed in an intersection region between the gate line and the data line and electrically connected to corresponding gate line and data line;

a plurality of storage capacitorsdisposed over the base plate, wherein each storage capacitor has an upper electrode having at least a first aperture, and the direction of the electric field adjacent to the first aperture being at a predetermined angle to an alignment direction of the liquid crystal molecules, the liquid crystal layer possessing a transition from a splay state to a bend state while operating ; and

a plurality of pixel electrodesdisposed over the pixel area, wherein each the pixel electrodes is respectively electrically connected to the corresponding active device and the corresponding upper electrode.

[c2] 2. The active device array structure of claim 1, wherein the gate lines are formedin parallel over the base plate, the data lines are formed in parallel over the base plate,and the gate lines are perpendicular to the date lines.

[c3] 3. The active device array structure of claim 1, wherein the active devices comprise thin film transistors.

[c4] 4. The active device array structure of claim 1, wherein the pixel electrodes comprise transparent electrodes.

[c5] 5. The active device array structure of claim 1, wherein the pixel electrodes comprise reflective electrodes.

[c6] 6. The active device array structure of claim 1, wherein the upper electrode is disposed over a portion of the gate line occupied area toform a storage capacitor.

[c7] 7. The active device array structure of claim 1, further comprises a plurality of common lines formed between the gate lines, and the upper electrode is disposed over a portion of the common line occupied area to form a

storage capacitor.

[c8] 8. The active device array structure of claim 1, wherein each of pixel electrodes further comprises at least a second aperture when the first aperture is located underneath the pixel electrode,and the second aperture is formed above the first aperture.